FULLY DIFFERENTIAL CMOS PHASE-LOCKED LOOP

CROSS-REFERENCES TO RELATED APPLICATION(S)

This application is a continuation of U.S. Patent Application Serial No. 09/919,636, which is a continuation-in-part application of U.S. Patent Application Serial No. 09/540,243, filed on March 31, 2000, now U.S. Patent No. 6,526,113 B1, which claims the benefit of priority from U.S. Provisional Patent Application Serial No. 60/148,417, filed on August 11, 1999, the disclosures of which are hereby incorporated by reference in its entirety for all purposes.

The continuation-in-part application U.S. Patent Application Serial No. 09/919,636 also claims the benefit of priority from U.S. Provisional Patent Application Serial No. 60/238,317 filed on October 4, 2000, the disclosure of which is also hereby incorporated by reference in its entirety for all purposes.

BACKGROUND OF THE INVENTION

The present invention relates in general to integrated circuits, and in particular to method and circuitry for implementing an improved phase-locked loop (PLL) in complementary metal-oxide-semiconductor (CMOS) technology.

The convergence of various high speed data communication technologies (e.g., Ethernet, fiber channel, IEEE firewire links) into the gigabit domain has focused the efforts of integrated circuit designers on developing high speed circuit techniques for processing broadband signals. Similarly, efforts directed at developing low cost and low power dissipation circuits have been driven by the explosive growth in wireless media for voice and data communications.

A circuit block that is commonly found in voice and data communication applications is a phase-locked loop (PLL). The primary function of the PLL is to maintain a fixed phase relationship between an input (e.g., clock) signal and a reference signal. A PLL designed for a digital application typically includes a phase and/or frequency detector, a charge pump, a loop filter, a voltage controlled oscillator (VCO), and an (optional) divider. The phase detector determines the phase differences between an input signal (i.e., an input data stream or an input clock) and a reference signal derived from the VCO, and generates a detector output signal indicative of the detected phase differences. The charge pump receives the detector output signal and generates a set of phase error signals (e.g., UP and DOWN currents fed into the filter). The

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loop filter filters the phase error signals to generate a control signal that is then used to adjust the frequency of the VCO such that the phases of the two signals provided to the phase detector are locked. When the phases of the two signals are locked, the respective frequencies of the two signals are exactly the same.

Fig. 1 is a simplified block diagram of a conventional phase locked loop 10. An input signal is provided to a phase detector 12 that also receives a reference signal from a divider 20. The input signal can be a clock signal, a data stream, or some other types of signal having phase and/or frequency information to which the phase locked loop can be locked. The reference signal is typically a clock signal used to trigger the phase detector 12. Phase detector 12 generates an output signal indicative of the timing differences (i.e., the phase differences) between the input signal and the reference signal. The output signal from the phase detector 12 is provided to a charge pump 14 that generates an output signal indicative of the detected phase error between the input and reference signals. In some designs, the charge pump output signal is logic high if the phase of the input signal is early (or late) relative to that of the reference signal, logic low if the phase of the input signal is late (or early) relative to that of the reference signal, and tri-stated for a period of time between clock edges.

The charge pump output signal is provided to a loop filter 16 that filters the signal with a particular transfer characteristic to generate a control signal. The control signal is then provided to, and used to control the frequency of, a voltage-controlled oscillator (VCO) 18. VCO 18 generates an output clock having a frequency can be adjusted by the control signal at the input of VCO. The output clock is provided to divider 20 that divides the frequency of the output clock by a factor of N to generate the reference signal. Divider 20 is optional and not used when the frequency of the output clock is the same as that of the input signal (i.e., N = 1). The control signal adjusts the frequency of VCO 18 such that the frequencies of the two signals provided to phase detector 12 are locked when the phase locked loop 10 is locked.

In typical PLLs, signals are transmitted between components in a non-differential manner. Signals transmitted in this manner, however, are subject to a number of shortcomings. For example, noise from power supply fluctuations and substrate can relatively easily affect the quality of such signals causing jitters and other problems. Hence, it would be desirable to implement the PLL in a fully differential architecture that would significantly reduce jitter and improve overall noise performance.

Furthermore, modern day devices and applications continually demand improved performance criteria including high speed, low power dissipation, and low cost, from their constituent components. To realize and meet such performance criteria, it would be desirable to implement the PLL in low-cost CMOS technology that allows for increased levels of integration.

SUMMARY OF THE INVENTION

The present invention relates specifically to a fully differential phase-locked loop. In one embodiment, the phase-locked loop includes a phase-frequency detector, a Gm cell block, a low pass filter and a voltage controlled oscillator. These various elements of the phase-locked loop are connected to one another in a fully differential manner, i.e., each element has an input and/or an output each having at least a differential signal. In one embodiment, each of these various elements of the phase-locked loop is implemented using high speed current-controlled complementary metal-oxide-semiconductor (C^3MOS) logic.

Accordingly, in an exemplary embodiment, an improved phase-locked loop is provided including: a detector configured to receive an input signal and a reference signal and to provide a detector output signal indicative of a difference between the input signal and the reference signal; a signal filter coupled to the detector and configured to receive the detector output signal and to provide a control signal; and a voltage controller oscillator coupled to the signal filter and configured to receive the control signal and to provide an oscillator signal which is adjustable based on the control signal, the oscillator signal is fed back to the detector as the reference signal; wherein the detector, the signal filter, and the voltage controller oscillator are connected to one another in a fully differential manner.

Optionally, a transconductance (or Gm) cell circuit is disposed between the detector and the signal filter and configured to provide a current output signal to the signal filter; and a divider circuit is disposed between the voltage controlled oscillator and the detector and configured to provide a divided version of the oscillator signal to the detector.

Accordingly, in another exemplary embodiment, a method for implementing a phase-locked loop having a plurality of components including a detector, a transconductance (or Gm) cell, a signal filter, a voltage controlled oscillator and a divider circuit is provided, comprising: connecting each of the plurality of components to one another in a differential manner; and implementing each of the plurality of components using C^3MOS logic.

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Reference to the remaining portions of the specification, including the drawings and claims, will realize other features and advantages of the present invention. Further features and advantages of the present invention, as well as the structure and operation of various embodiments of the present invention, are described in detail below with respect to accompanying drawings, like reference numbers indicate identical or functionally similar elements.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a simplified schematic block diagram of a conventional phase locked loop;

Fig. 2 is a simplified schematic block diagram of a phase locked loop according to one exemplary embodiment of the present invention;

Fig. 3 is a simplified schematic block diagram of a differential phase-frequency detector according to one exemplary embodiment of the present invention;

Fig. 4 is a simplified circuit diagram of a differential Gm cell block according to one exemplary embodiment of the present invention; and

Fig. 5 is a simplified schematic block diagram of a differential voltage controlled oscillator according to one exemplary embodiment of the present invention.

DESCRIPTION OF THE SPECIFIC EMBODIMENTS

The present invention will now be described. Referring to Fig. 2, there 20 is shown a simplified schematic block diagram of a PLL 100 according to one exemplary embodiment of the present invention. According to this exemplary embodiment, PLL 100 is fully differential and is implemented in standard CMOS processing technology using current-controlled CMOS (or C^3MOS) logic. Using C^3MOS logic allows for higher degree of integration which, in turn, leads to high 25 speed signal processing and lower cost.

Various embodiments for circuitry implemented using C^3MOS logic are described in detail in commonly-assigned U.S. Patent Application Serial No. 09/484,856, entitled "Current-Controlled CMOS Logic Family," to A. Hairapetian, filed on January 18, 2000, now U.S. Pat. No. 6,424,194 B1, which is hereby incorporated by reference for all purposes. As described therein, the basic building block of the C^3MOS logic family uses a pair of conventional

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MOSFETs that steer current between a pair of load devices in response to a difference between a pair of input signals. Thus, unlike conventional CMOS logic, C^3MOS logic dissipates static current and is able to operate at much higher speeds.

The C^3MOS logic family contains all the building blocks of other logic families. Examples of such building blocks include inverters, buffers, level shift buffers, N-input NOR and NAND gates, exclusive OR (XOR) gates, flip flops and latches, and the like. More complex logic circuits such as shift registers, counters, frequency dividers, etc., can be constructed in C^3MOS using the basic logic elements. Based on the disclosure and teaching provided in U.S. patent application number 09/484,856, as identified above, it should be apparent to a person of ordinary skill in the art to be able to use C^3MOS logic to design complex logic circuits.

As shown in Fig. 2, in an exemplary embodiment, the PLL 100 includes a differential input buffer BUFF 102, a differential phase-frequency detector PFD 104, a Gm cell block 106, a low pass filter 108, a voltage controller oscillator VCO 110 and a divider 112. As will be further described below, these various elements of the PLL 100 are connected to one another in a fully differential manner. In other words, each of the elements of the PLL 100 has at least a differential input comprising two constituent input signals and a differential output comprising two constituent output signals. It should be understood that a differential signal inherently includes two constituent signals.

The PLL 100 receives a differential input signal, including two input clock signals REFCKP and REFCKN, at the differential input buffer 102. The differential input buffer 102 amplifies and conditions the two input clock signals REFCKP and REFCKN while maintaining their differential nature. The differential input buffer 102 is preferably implemented in C^3MOS logic. By implementing the differential input buffer 102 in C^3MOS, good common mode rejection and high slew rate earl be achieved. The use of buffer 102, however, is optional.

The differential phase-frequency detector 104 then receives the differential input signal as well as a differential reference signal, including signals FBCKN and FBCKP, from the differential input buffer 102 and the divider 112 respectively. The phase-frequency detector 104 detects the difference, if any, in the phase/frequency of the differential input clock signal and the differential reference signal and accordingly generates two differential detector output signals comprising two pairs of output signals in the form of complementary UP or DN signals. It should be noted that each of the complementary UP and DN differential signals is made up of a pair of signals UP/UPB and DN/DNB respectively.

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Fig. 3 shows an exemplary implementation for the differential phase-frequency detector 104. In this exemplary implementation, the differential phase-frequency detector 104 includes a pair of resetable flip-flops RFF 200 and 202, a chain of buffers 206 and an AND logic function implemented in the form of an AND gate 204. Preferably, these various circuit elements in the differential phase-frequency detector 104 are implemented using C^3MOS logic.

Resetable flip-flops 200 and 202 receive differential signals at REFP/REFN and FBP/FBN inputs from the differential input buffer 102 and the divider 112, respectively. AND gate 204 then logically combines the four outputs UP/UPB and DN/DNB from the two resetable flip-flops 200 and 202 to generate the reset signal RST which is eventually fed back to the two flip-flops 200 and 202. The chain of buffers 206 add a pre-determined amount of delay before the reset signal RST is applied to the flip-flops 200 and 202 to avoid a too narrow reset signal RST.

Referring back to Fig. 2, the differential detector output signals from the phase-frequency detector 104 are then fed to the Gm cell block 106. The Gm cell block 106 operates to convert a voltage input signal to a current output signal which is indicative of the detected phase/frequency error, if any, between the two differential signals received by the differential phase-frequency detector 104. A pre-filter may be optionally included between the outputs of the phase-frequency detector 104 and the inputs of the Gm cell 106 to adjust signal levels for C^3MOS logic levels, if desired.

Fig. 4 is an exemplary circuit implementation for a fully differential Gm cell block 106. Under this exemplary implementation, the Gm cell block 106 includes an amplifier stage 300 made up of a pair of differential inputs that receives signals DN/DNB and UP/UPB from the differential phase-frequency detector 104, and current source and load devices. More specifically, the amplifier stage 300 is connected to a common-mode feedback (CMFB) circuit 302. Preferably, the Gm cell block 106 is fully differential and is implemented using C^3MOS technology. Detailed description of one embodiment of a Gm cell block 106 for use in the PLL 100 of the present invention is provided in commonly assigned U.S. Patent Application Serial No. 09/540,243, entitled "Gm cell based Phase Locked Loops," by Gutierrez et al., filed on 3/31/00, now U.S. Pat. No. 6,526,113 B1, which is hereby incorporated in its entirety.

Referring back to Fig. 2, the Gm cell block 106 combines with the low pass filter LPF 108 to form an ideal integrator. The low pass filter 108 is a differential filter made of, for

example, an RC network that can be either integrated with the rest of the circuitry or placed off chip. Since the output of the Gm cell block 106 is a differential current signal, feeding the output of the Gm cell block 106 to the low pass filter 108 causes voltage potential to develop at signals VCP and VCN which represent a differential voltage signal.

The differential voltage signal, represented by VCP and VCN, at the output of the Gm cell block 106 are then applied to the differential voltage controlled oscillator 110 to control the frequency of a differential oscillator output which is comprised of signals CLKP and CLKN. When the PLL 100 is locked, the voltage controlled oscillator 110 generates a differential oscillator output having a frequency that is locked to that of the differential input signal, REFCKP and REFCKN.

Fig. 5 is a simplified schematic block diagram showing an exemplary implementation of the fully differential voltage controlled oscillator 110. As shown in Fig. 5, the voltage controlled oscillator 110 is implemented in the form of a differentially tuned varactor-inductor oscillator. Such an exemplary oscillator is described in greater detail in commonly assigned U.S. Patent Application Serial No. 09/792,684, filed on 02/24/01, entitled "Method and Circuitry for Implementing a Differentially Tuned Varactor-Inductor Oscillator," to Gutierrez, which is hereby incorporated by reference in its entirety.

The differential oscillator output of the voltage controlled oscillator 110 is then fed to divider 112, if necessary. Since the voltage controlled oscillator 110 usually operates at a high frequency, e.g., 32 times the input signal frequency, the frequency of the differential oscillator output may need to be reduced before it is provided to the phase-frequency detector 104. The divider 112 is used for this frequency-reduction purpose.

The divider or divide by N (÷N) circuit 112 receives the differential oscillator output of the voltage controlled oscillator 110. The divider 112 then divides the signal frequency down to the input frequency (e.g., ÷32), generating signals FBCKN and FBCKP, which represent a divided version of the differential oscillator output, which are fed back to the phase-frequency detector 104. Preferably, the divider 112 is also implemented using differential C^3MOS logic.

As thus constructed, a fully differential PLL using C^3MOS logic exhibits a number of performance advantages over prior art PLLs including higher speed, reduced noise and ease of integration.

It is understood that the examples and embodiments described herein are for illustrative purposes only and that various modifications or changes in light thereof will be suggested to persons skilled in the art and are to be included within the spirit and purview of this application and scope of the appended claims. All publications, patents, and patent applications cited herein are hereby incorporated by reference for all purposes in their entirety.